IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:		§		
	Paul Petersen	§	Group Art Unit:	2189
		§		
Serial No.:	09/419,523	§		
		§	Examiner:	Peikari, Behzad
Filed:	October 18, 1999	§		
		§		
For:	DETERMINING MEMORY UPGRADE OPTIONS	§	Atty. Docket:	MICS:0188 FLE/MAN (99-2108.00)

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Sir:

REQUEST FOR REHEARING

This Request for Rehearing is being filed in response to the Decision on Appeal mailed on April 27, 2009.

The Appellant files this Request for Rehearing to address certain statements made by the Board of Patent Appeals and Interferences in the Decision on Appeal. More specifically, the Appellant will state with particularity the points believed to have been misapprehended or overlooked by the Board. As further addressed in detail below, the Appellant respectfully notes that at least a portion of the Board's misapprehension is likely related to the Board's decision to not consider pages 1-7 of the Reply Brief, based on an asserted waiver relating to issues not purportedly raised in the principal Brief. However, as discussed below, only a single paragraph of pages 1-7 of the Reply Brief was directed to the issue that the Board asserted was untimely for failure to raise the issue in the principal Brief (i.e., the "combinability argument").

On page 6, lines 1-30 of the Board's opinion, the Board enters statements made on pages 10 and 11 of the Examiner's Answer as findings in fact. These statements include, *inter alia*, "As for 'executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system,' this was a well known technique used to determine total memory capacity in prior art systems and was 'readily understood by one of ordinary skill in the art,' as conceded by appellant on page 10 of the Appeal Brief." The point overlooked was made to the Board in the Reply Brief, page 4, lines 1-15. Specifically, in response to the Examiner's assertion, the Appellant timely noted that such a concession was *not* made by the Appellant. The Examiner has taken the statement of "readily understood by one of ordinary skill in the art" *out of context* and has manipulated the description to conveniently fit the Examiner's argument. In fact, when read in context, the statement "readily understood by one of ordinary skill in the art" *clearly refers* to the preceding portion of the statement relating to reading information from a non-volatile storage device. That is, the only point conceded by the Appellant is the fact that reading information from a non-volatile storage device is readily understood by those skilled in the art, *not* that executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system was known. Accordingly, the Appellant asserts that entering the concession as a finding of fact was improper. The Appellant does not concede that the aforementioned claim limitation is well known, and in fact, the Appellant traverses such an assertion.

On page 7, lines 19-25 of the Board's opinion, the Board states that they do not agree with the Appellant's urgings that "the combination of teachings of Arai and Yoshizawa does not teach the ability to determine the maximum of number of memory devices at any point in time that 'can' be supported by a memory channel and by a respective controller to include device sockets to which they are attached." The point overlooked was made to the Board in the principal Brief page 11, line 23 to page 12, line 6 and further articulated in the Reply Brief, page 2, line 6 to page 3, line 23 and the Reply Brief, page 4, line 17 to page 5, line 17. The response is that both Arai and Yoshizawa fail to teach such limitations. Arai teaches the setting of expanded and extended memory configurations (which relate to techniques for *addressing* available memory) and requires the user to enter the desired "capacities" of each configuration (where capacity refers solely to the

capacity refers solely to the desired amount of *installed* memory a user wishes to utilize for each configuration). It fails to teach determining the total memory capacity of the system, instead dealing only with the allocation of installed memory. Yoshizawa teaches a system and method for enabling memory expansion without shutting off the computer by detecting changes in the amount of installed memory. It also fails to teach determining the total memory capacity of the system, dealing only with the detection of *previously installed* or *currently installed* memory. This difference is significant. Whereas the Appellant's claims provide for determining the memory capacity of the system (i.e., how much memory can be installed into the system), each of the cited references disclosed determining how much memory is in fact installed into the system. As such, both references fail to teach "determining a maximum number of memory devices that can be supported per memory bus channel" and "determining a maximum number of device sockets that can be supported by a memory controller," and thus fail to teach all of the claim limitations in the present invention.

On page 7, line 25 to page 8, line 3 of the Board's opinion, the Board states "Furthermore, the Examiner's responsive arguments in finding of fact 2 are extensive and amplify the corresponding teaching in Ware (RAMBUS) which are not contested in the Reply Brief." The point overlooked was made to the Board in the Reply Brief, page 5, lines 4-17. The response is that the Appellant did contest the Examiner's discussion of RAMBUS in stating that "the Examiner merely discusses RAMBUS in the context of determining whether a device is present or not. Further, the RAMBUS data sheet relied on by the Examiner fails to teach or suggest any configuration that indicates the maximum number of device sockets that *can* be supported by the memory controller." The Reply Brief goes on to state that "the claims recite determining a number of memory devices or sockets that can be supported by the system and, in contrast, the Arai reference discloses merely allocating memory based on the memory that is actually installed in the system, Yoshizawa merely discloses a system and method of swapping installed memory, and RAMBUS merely addresses what is currently installed. None of the three references determine the potential capabilities of the system, but instead are based on what is actually installed in the system." Thus, the Appellant did contest the Examiner's arguments in the Reply Brief.

On page 8, lines 4-9 of the Board's opinion, the Board states that the arguments presented from page 1 through the middle of page 7 of the Reply Brief will not be considered as the arguments are considered "untimely and have essentially been waived since the combinability argument has not been raised initially in the principal Brief on appeal." The point overlooked was made to the Board in the principal Brief, page 11, line 23 to page 13, line 3, and further articulated in the Reply Brief, page 2, line 6 to page 5, line 17 and page 6, line 9 to page 7, line 7. The response is that the principal Brief argues that the references cited by the Examiner do not teach all of the claim limitations and that the majority of arguments raised on pages 1 through 7 of the Reply Brief rearticulate this position. The only portion of the Reply Brief dealing with the "combinability argument" may be found on page 5, line 18 to page 6, line 8. Thus, at most only this *one paragraph* should have been ignored by the Board. It was improper for the Board not to consider the remaining arguments in the Reply Brief as they were properly raised in the principal Brief.

On page 8, lines 10-13 of the Board's opinion, the Board states that the arguments presented at pages 7 and 8 of the Reply Brief are misplaced since "the combinability of the teachings of Arai and Yoshizawa has already been determined to be proper within 35 U.S.C. § 103 from [the] prior decision, including for the present claims on appeal." The point misapprehended was made to the Board in the Reply Brief, page 7, line 12 to page 8, line 25. The response is that the arguments presented on these pages do not deal with the combinability of the teachings of Arai and Yoshizawa. The arguments deal with the Examiner's assertion that some of the *appealed claims are simply combinations of prior claims* that the Board has already considered. The Appellant cited evidence that this was not the case (by showing additional limitations in the claims not previously presented to the Board) and pointed to inconsistencies in the Examiner's statements (by emphasizing that the Examiner admitted new limitations existed in the Examiner's Answer). The Appellant is unsure why these arguments were considered misplaced by the Board and what relation they have to a determination that the combinability of the teachings of Arai and Yoshizawa is proper.

On page 8, lines 16-18 of the Board's opinion, the Board states that the Examiner "properly referred to admissions made by Appellant at the bottom of page 10 of the principal Brief on Appeal." As was stated previously, the point overlooked was made to the Board in the Reply Brief, page 4, lines 1-15, as well as in the Reply Brief, page 9, lines 1-10. The response is that the Appellant did not make such an admission.

On page 8, lines 22-25 of the Board's opinion, the Board states "What is very telling in these remarks in this portion of the Reply Brief is the failure to consider all the arguments that we reproduced from the Examiner in finding of fact 2." As was stated previously, the point overlooked was made to the Board in the Reply Brief, page 5, lines 4-17. The response is that the Appellant did consider and address the Examiner's discussion of RAMBUS when saying that "the Examiner merely discusses RAMBUS in the context of determining whether a device is present or not. Further, the RAMBUS data sheet relied on by the Examiner fails to teach or suggest any configuration that indicates the maximum number of device sockets that *can* be supported by the memory controller." Since the RAMBUS reference *as a whole* fails to teach the limitation, the Appellant did not need to refute each statement individually.

Conclusion

Based upon the above points of clarification in conjunction with the arguments made in the Appeal Brief and Reply Brief, the Appellant believes that the claims are clearly allowable over the cited art. The Examiner's rejections, therefore, cannot stand.

Respectfully submitted,

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/Robert A. Manware/
Robert A. Manware
Reg. No. 48,758
FLETCHER YODER
P.O. Box 692289
Houston, TX 77269-2289
(281) 970-4545